Notice of Allowability	Application No.	Applicant(s)	
	10/728,965	OSADA ET AL.	
	Examiner	Art Unit	
	VanThu Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Response to Election / Restriction Filed filed on 7/13/05*.

2. ☒ The allowed claim(s) is/are *1-9*.

3. ☒ The drawings filed on *08 December 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 12/08/2003
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☒ Other Search history

VanThu Nguyen
Primary Examiner
Art Unit: 2824

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

For Claims:

Cancel claims 10-18.

In claims 2-9, replace "A" with --The-- on line 1 of each claim.

For Abstract:

Replace "According to one aspect of the present invention, there is provided a semiconductor device comprising" with --A semiconductor device comprises--.

2. The following is an examiner's statement of reasons for allowance:

The following is a statement of reasons for the indication of allowance:

The prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Kono (6,714,471), Sato et al. (6,026,014), and Ohsawa (4,748,627), taken individually or in combination, do not teach the claimed invention having limitations as in claim 1.

Kono discloses a semiconductor device (10, see FIG. 1) comprising a plurality of bit-line pairs (plurality of BL and /BL, see FIG. 2); a plurality of inherent word lines; a plurality of inherent memory cells provided at intersection points formed by the plurality of bit-line pairs and the plurality of word lines; a plurality of sense amplifiers (SENSE AMPLIFIER (SA) 50s, see

FIG. 1), each of which is provided for each given number of bit-line pairs from among the plurality of bit-line pairs (each SENSE AMPLIFIER (SA) 50 corresponding to each banks 52, BANK #0 TO BANK #3, see FIG. 1); a plurality of write amplifiers (PREAMPLIFIER (PA) & WRITE AMPLIFIER 48s, see FIG. 1), each of which is provided for said each given number of bit-line pairs (each PREAMPLIFIER (PA) & WRITE AMPLIFIER 48 corresponding to each banks 52, BANK #0 TO BANK #3, see FIG. 1); a control circuit (CONTROL CIRCUIT 42 and COLUMN DECODER 46, see FIG. 1) that selectively connects one of the given number of bit-line pairs to the sense amplifier, and that selectively connects one of the given number of bit-line pairs to the write amplifier; an address storing circuit (ADDRESS BUFFER 26) for storing an address corresponding to the data to write.

Sato disclose a semiconductor device (see FIG. 14) comprising data storing circuit (D.L.U. and D.L.D, see FIG. 1).

Ohsawa discloses, in FIG. 1, a semiconductor device comprising a plurality of memory arrays inherently comprising bit lines, word lines, and memory cells; an error-correction circuit (DECODING/CORRECTION CIRCUIT 19) corrects an error of data read out corresponding to a writing address, and then generates first data to write (see Abstract)

However, neither Kono, Sato et al. nor Ohsawa teaches the semiconductor writes the first data to the memory cell via the write amplifier, after a second writing address is inputted into the address storing circuit.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (571) 272-1881. The examiner can normally be reached on Monday-Friday, 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

August 6, 2005

VanThu Nguyen
Primary Examiner
Art Unit 2824